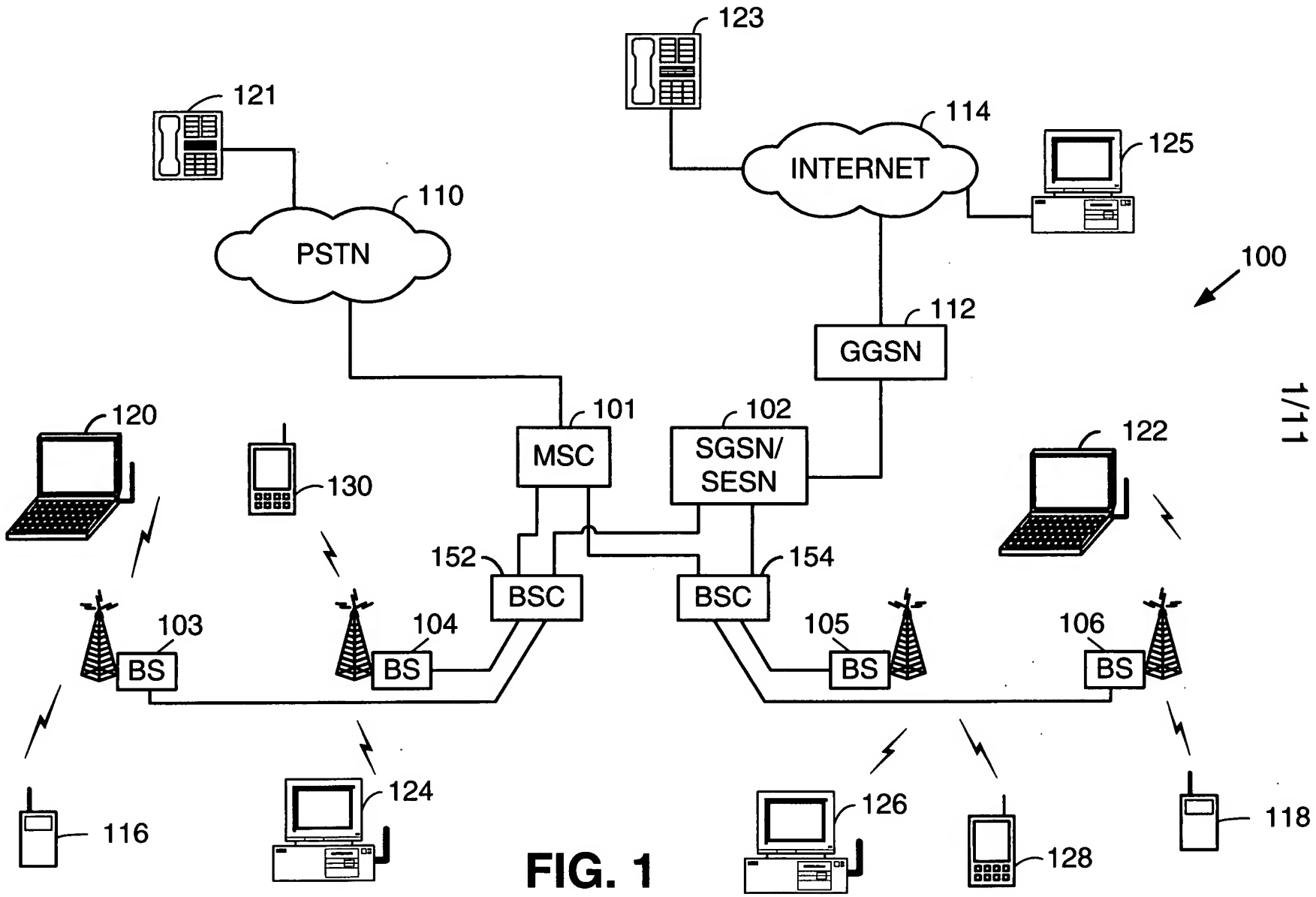
123
121
114
INTERNET
125
110
PSTN
100
112
GGSN
101
102
MSC
SGSN/
SESN
120
130
122
152
154
BSC
BSC
103
104
105
106
BS
BS
BS
BS
124
126
116
128
118

FIG. 1

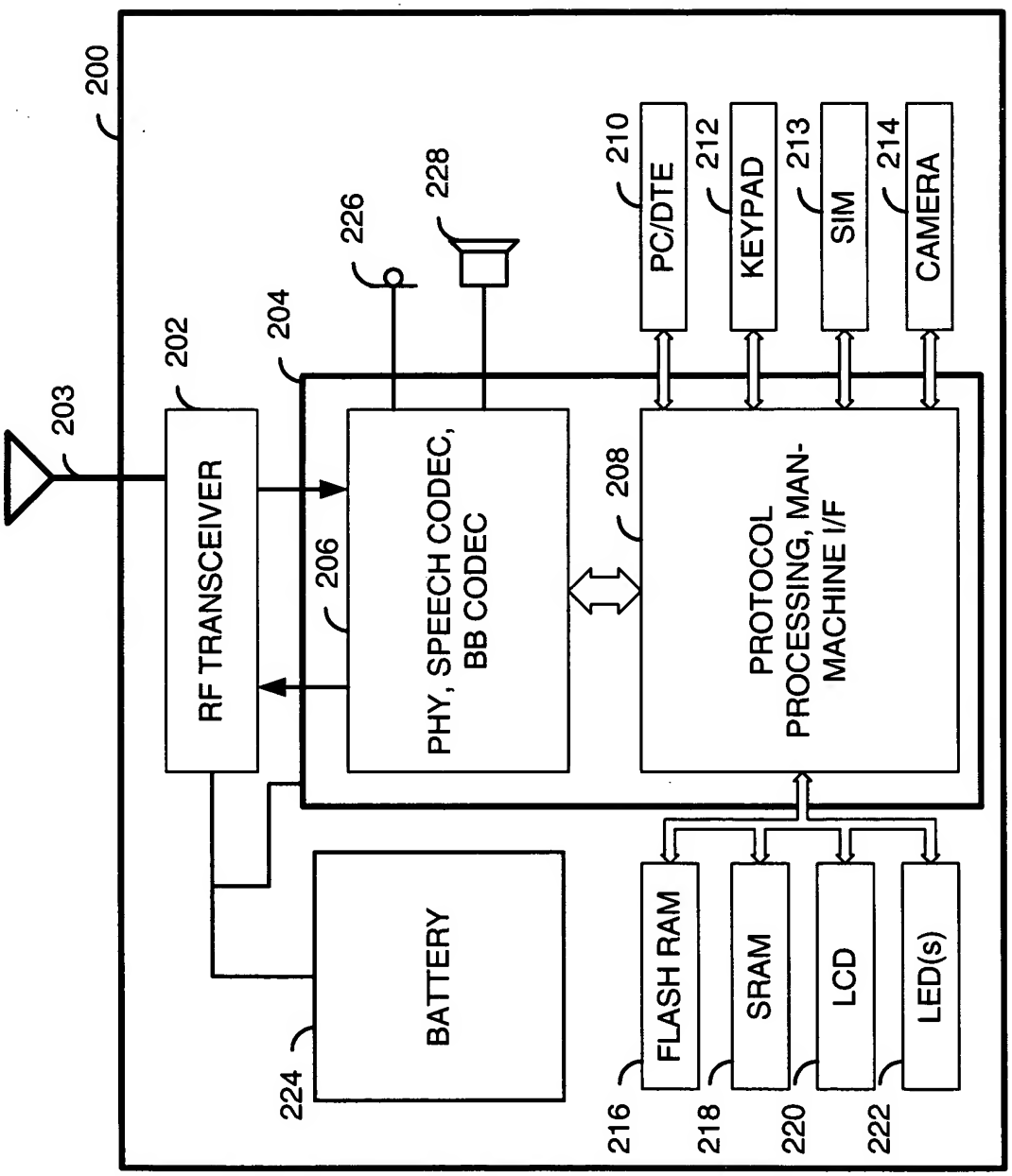
200
203
202
RF TRANSCEIVER
204
206
PHY, SPEECH CODEC, BB CODEC
208
PROTOCOL PROCESSING, MAN-MACHINE I/F
210
PC/DTE
212
KEYPAD
213
SIM
214
CAMERA
226
228
224
BATTERY
216
FLASH RAM
218
SRAM
220
LCD
222
LED(s)

FIG. 2

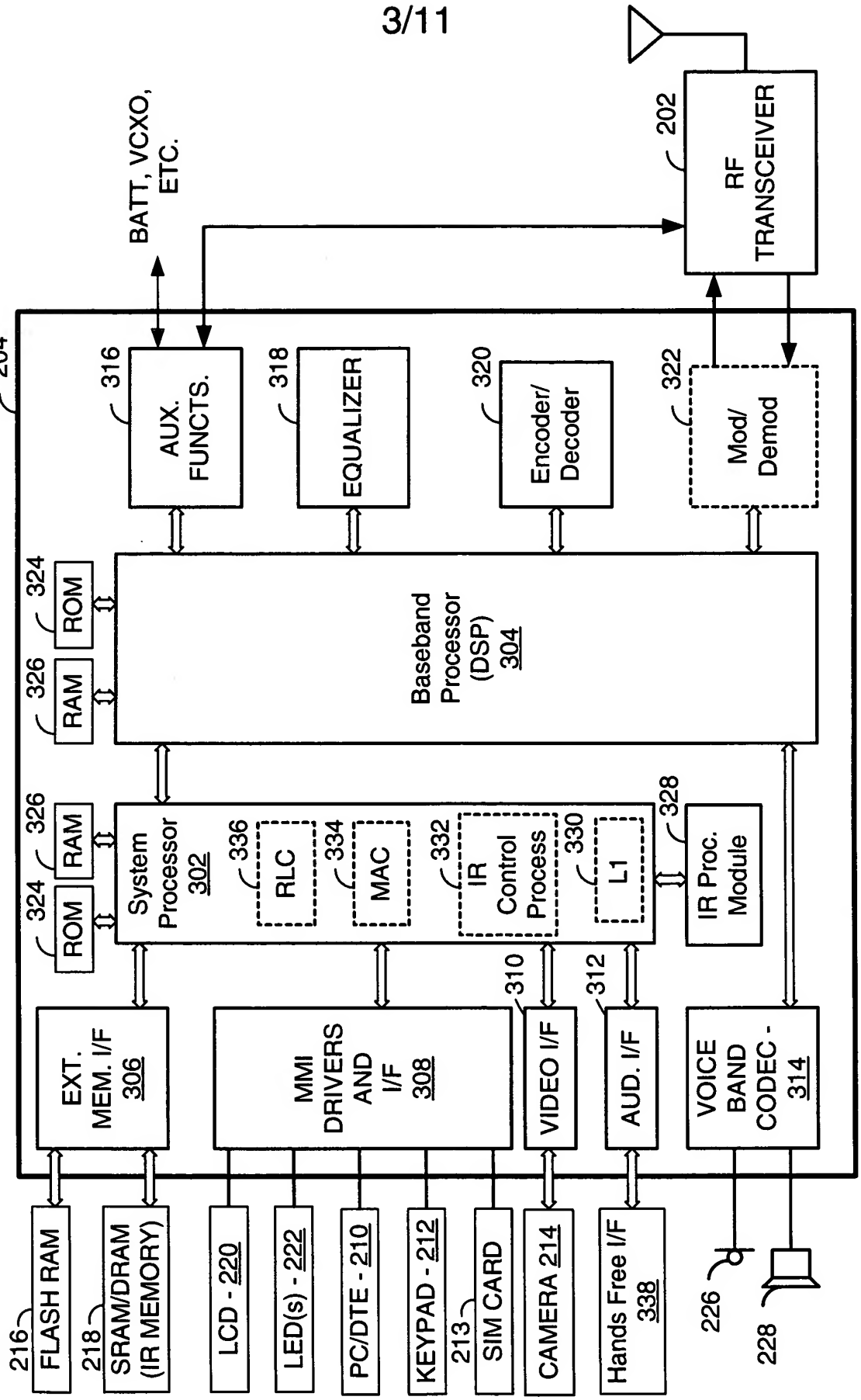
BATT, VCXO, ETC.
202
RF TRANSCEIVER
204
316
AUX. FUNCTS.
318
EQUALIZER
320
Encoder/ Decoder
322
Mod/ Demod
324
ROM
326
RAM
Baseband Processor (DSP) 304
326
RAM
324
ROM
System Processor 302
336
RLC
334
MAC
332
IR Control Process
330
L1
328
IR Proc. Module
EXT. MEM. I/F 306
MMI DRIVERS AND I/F 308
310
VIDEO I/F
312
AUD. I/F
VOICE BAND CODEC - 314
216
FLASH RAM
218
SRAM/DRAM (IR MEMORY)
LCD - 220
LED(s) - 222
PC/DTE - 210
KEYPAD - 212
213
SIM CARD
CAMERA 214
Hands Free I/F 338
226
228
200

FIG. 3

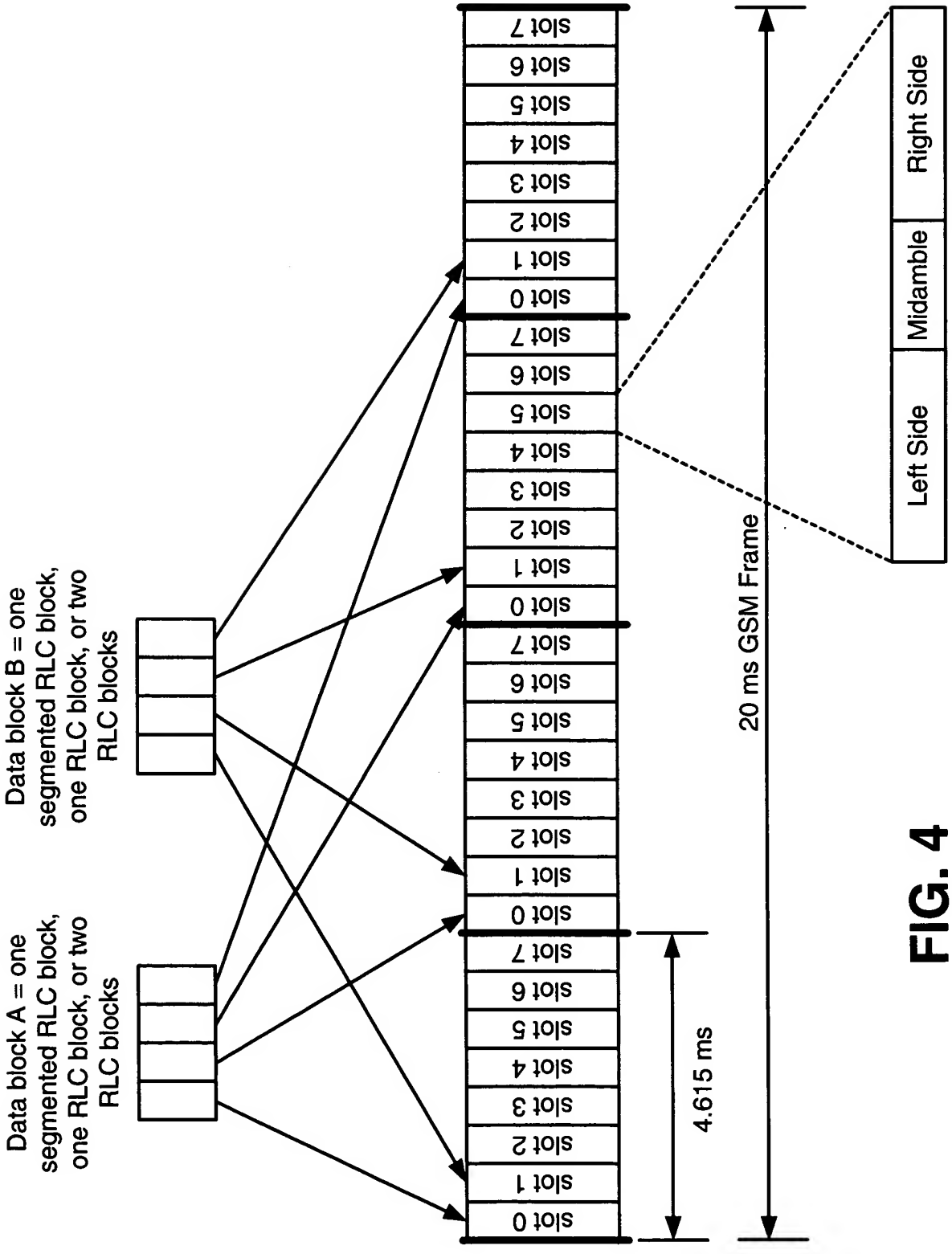
Data block A = one segmented RLC block, one RLC block, or two RLC blocks
Data block B = one segmented RLC block, one RLC block, or two RLC blocks
slot 0
slot 1
slot 2
slot 3
slot 4
slot 5
slot 6
slot 7
4.615 ms
20 ms GSM Frame
Left Side
Midamble
Right Side

FIG. 4

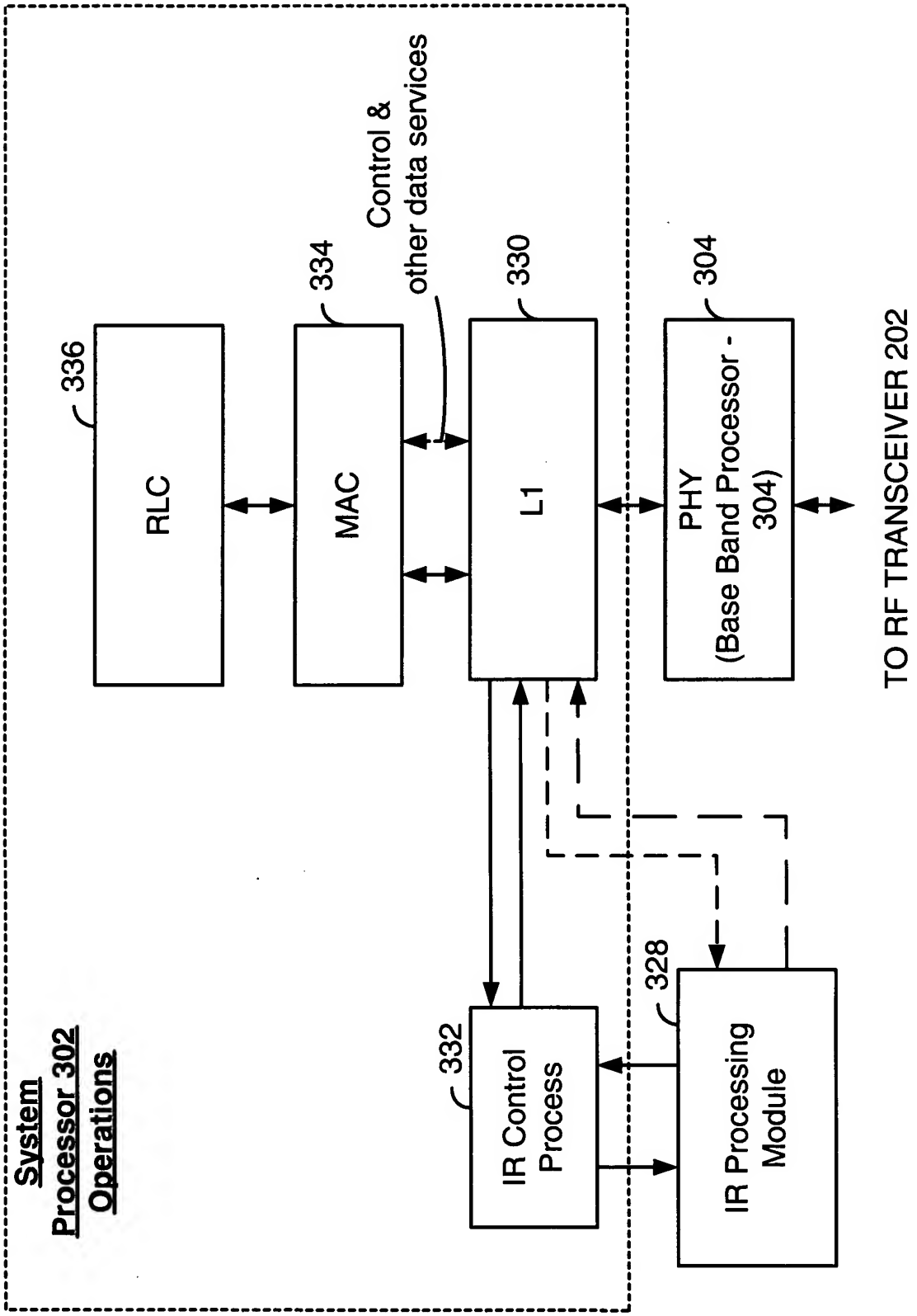
System
Processor 302
Operations
RLC
336
MAC
334
Control &
other data services
L1
330
PHY
(Base Band Processor -
304)
304
TO RF TRANSCEIVER 202
IR Control
Process
332
IR Processing
Module
328

FIG. 5A

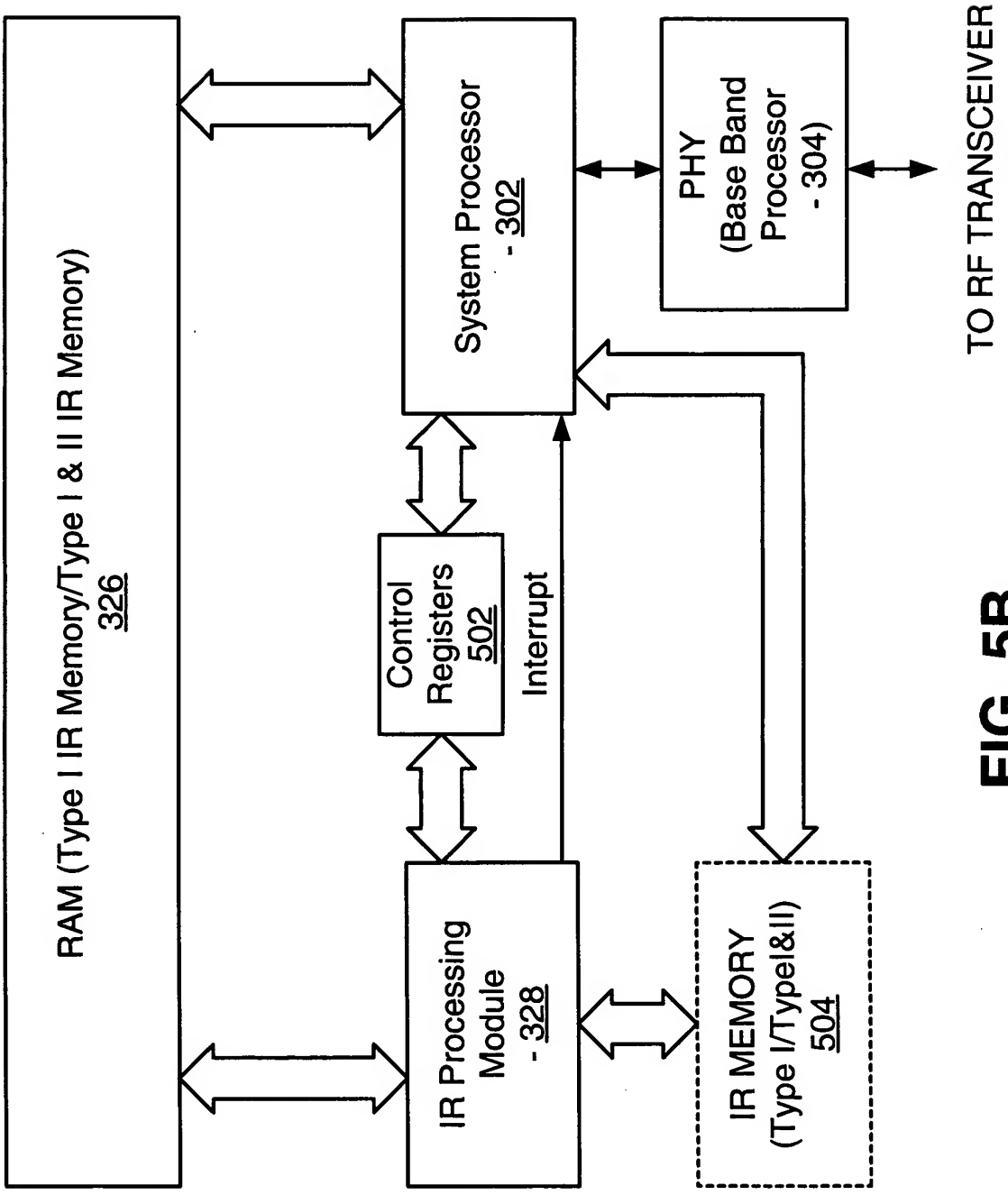
RAM (Type I IR Memory/Type I & II IR Memory)
326
System Processor
- 302
PHY
(Base Band
Processor
- 304)
TO RF TRANSCEIVER
Control
Registers
502
Interrupt
IR Processing
Module
- 328
IR MEMORY
(Type I/TypeI&II)
504

FIG. 5B

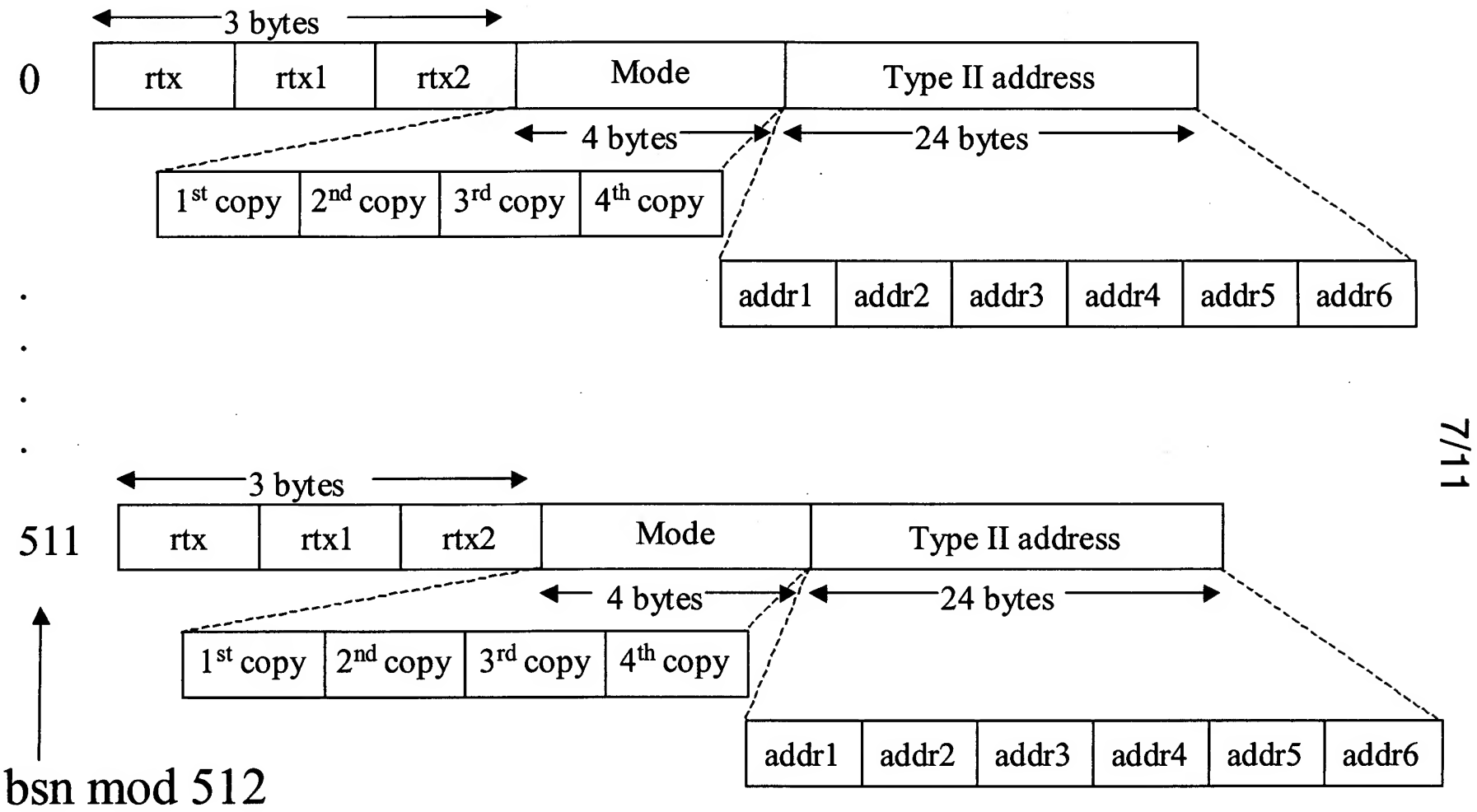
3 bytes
0
rtx
rtx1
rtx2
Mode
Type II address
4 bytes
24 bytes
1st copy
2nd copy
3rd copy
4th copy
addr1
addr2
addr3
addr4
addr5
addr6
3 bytes
511
rtx
rtx1
rtx2
Mode
Type II address
4 bytes
24 bytes
1st copy
2nd copy
3rd copy
4th copy
addr1
addr2
addr3
addr4
addr5
addr6
bsn mod 512

FIG. 6

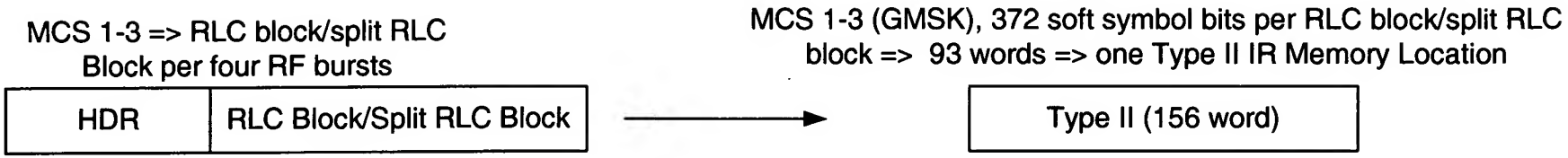

FIG. 7A

FIG. 7B

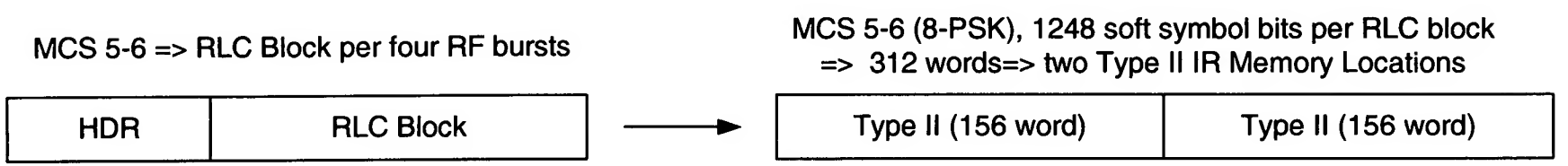

FIG. 7C

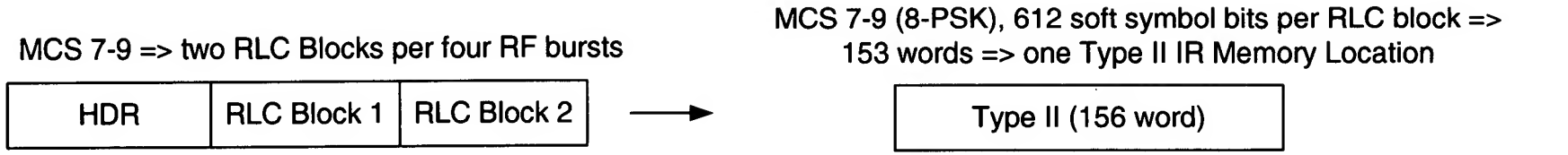

FIG. 7D

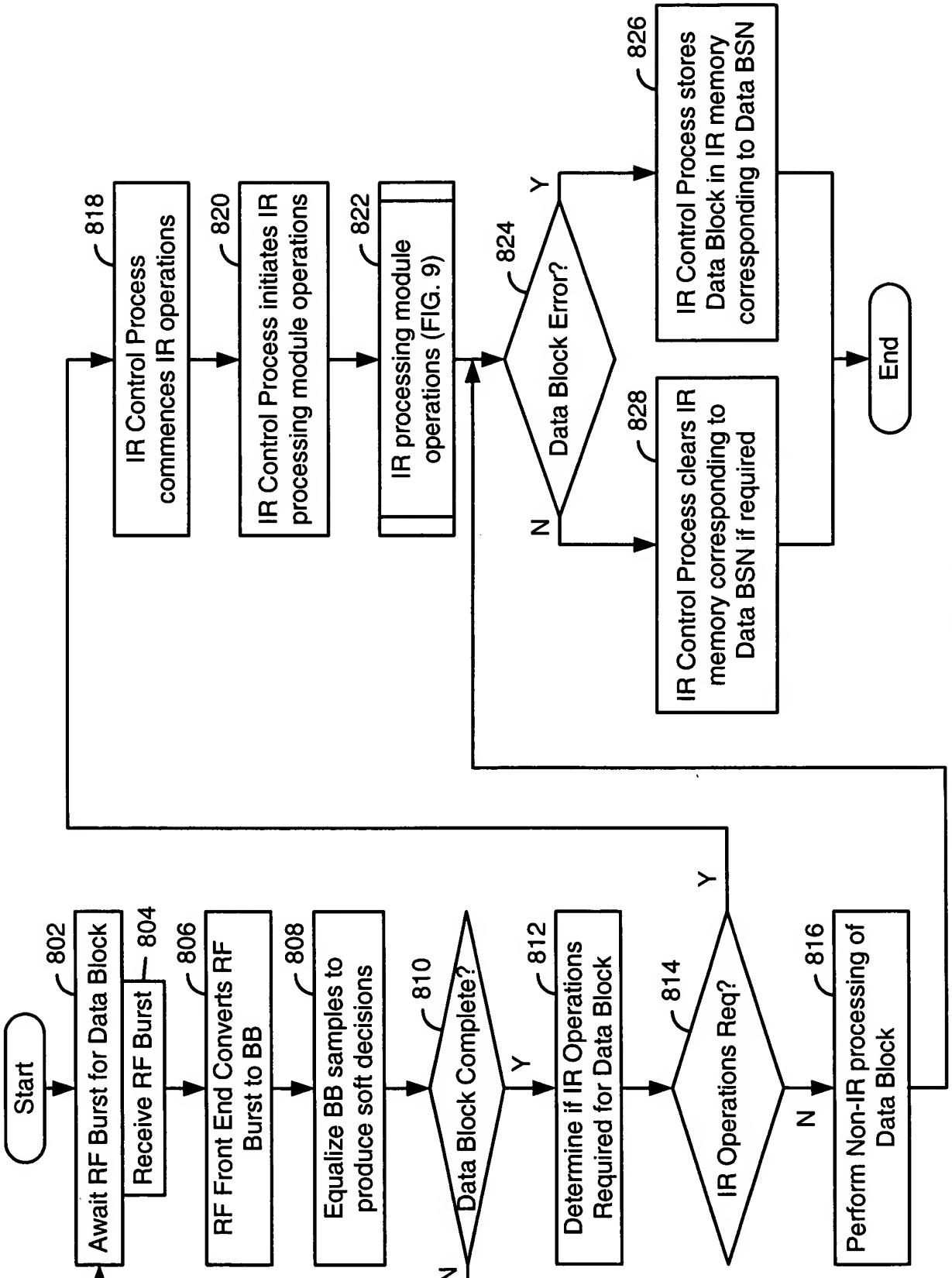
Start
802
Await RF Burst for Data Block
804
Receive RF Burst
806
RF Front End Converts RF Burst to BB
808
Equalize BB samples to produce soft decisions
810
Data Block Complete?
N
Y
812
Determine if IR Operations Required for Data Block
814
IR Operations Req?
N
Y
816
Perform Non-IR processing of Data Block
818
IR Control Process commences IR operations
820
IR Control Process initiates IR processing module operations
822
IR processing module operations (FIG. 9)
824
Data Block Error?
N
Y
826
IR Control Process stores Data Block in IR memory corresponding to Data BSN
828
IR Control Process clears IR memory corresponding to Data BSN if required
End

FIG. 8

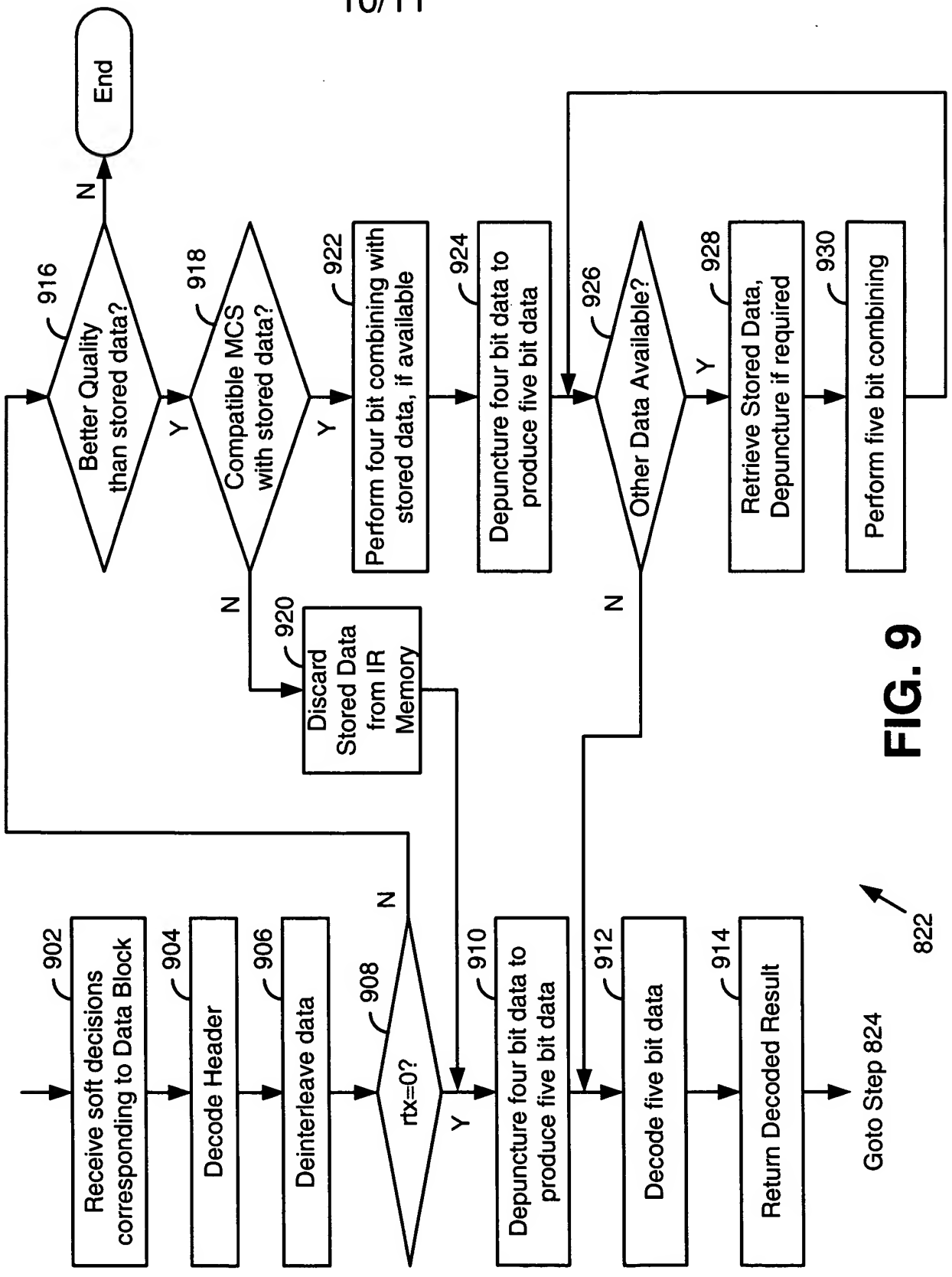
Receive soft decisions corresponding to Data Block
902
Decode Header
904
Deinterleave data
906
rtx=0?
908
N
Y
Depuncture four bit data to produce five bit data
910
Decode five bit data
912
Return Decoded Result
914
Goto Step 824
822
Discard Stored Data from IR Memory
920
N
Compatible MCS with stored data?
918
Y
Perform four bit combining with stored data, if available
922
Depuncture four bit data to produce five bit data
924
Other Data Available?
926
N
Y
Retrieve Stored Data, Depuncture if required
928
Perform five bit combining
930
Better Quality than stored data?
916
Y
N
End

FIG. 9

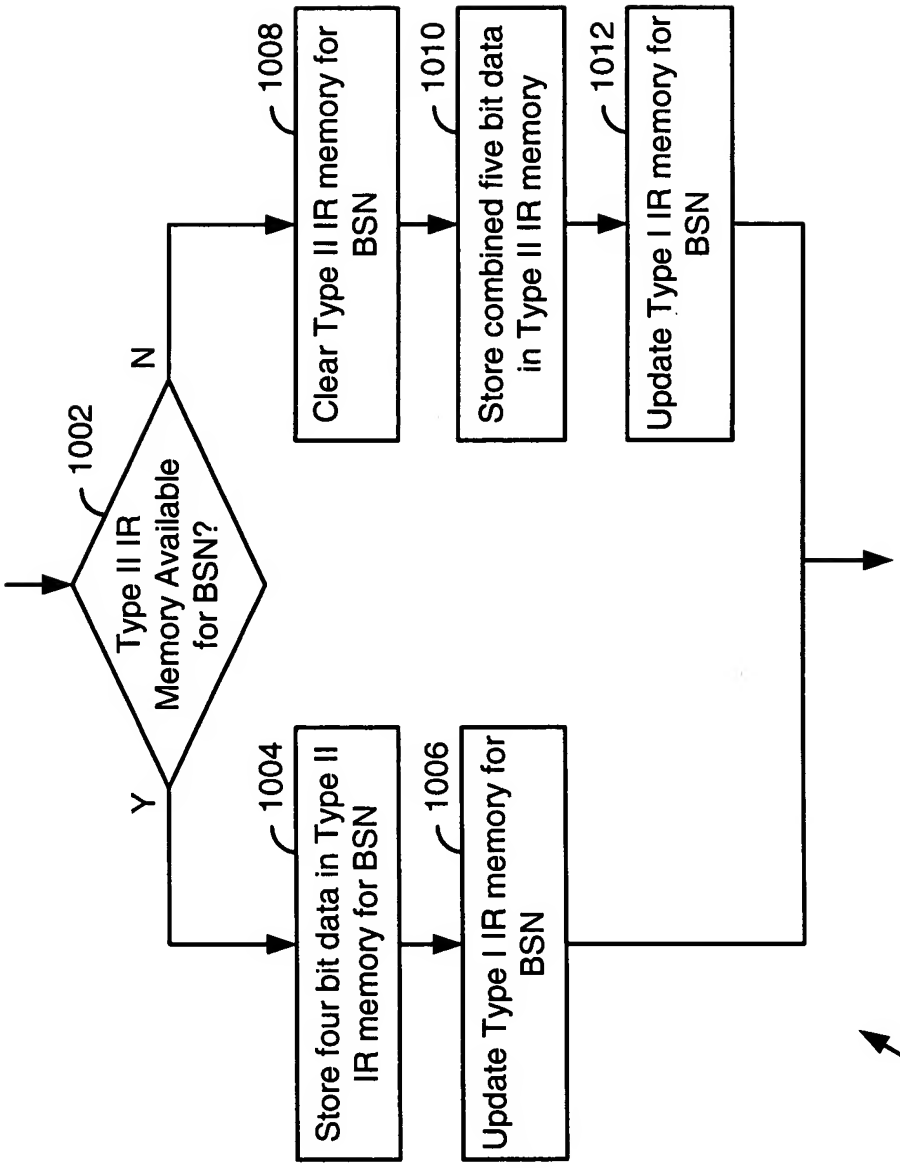
1002
Type II IR Memory Available for BSN?
N
Y
1008
Clear Type II IR memory for BSN
1010
Store combined five bit data in Type II IR memory
1012
Update Type I IR memory for BSN
1004
Store four bit data in Type II IR memory for BSN
1006
Update Type I IR memory for BSN
826

FIG. 10